even extending it as far as the field plate dielectric **18** at the maximum applicable blocking voltage at the semiconductor device **1**.

[0015] In one embodiment of this arrangement, avoiding sharp radii of curvature of the equipotential lines and/or equipotential surfaces in the transition region **30** from the cell field **9** to the edge region **12**, can be achieved by varying the compensation. To this end the degree of compensation, i.e., the difference between the p- and n-dopant dosages, is switched from an almost fully compensated state in the cell field **9** to a reduction in the p-dopant dosages towards the edge region **12**. In one embodiment, this may be achieved by reducing the width b of the charge compensation zones **22**, which are positioned approximately equidistant from one another in the cell field **9** with a predetermined stepwidth P and have a width b_z in the cell field **9**, from a width b_1—which corresponds approximately to width b_z—via b_2 to b_3. This prevents high peaks of electrical field strength forming at extreme curves in the equipotential lines **25/31** at the transition **30** from the cell field **9** to the edge region **12** and causing a premature avalanche break-through.

[0016] In one embodiment, therefore, a capacitance substantially independent of the voltage V_{DS} is monolithically integrated in and on the semiconductor body **6** beneath the gate bond contact area **13** with the aid of the field plate **15** in such a manner that the voltage is reduced to almost zero over the field plate dielectric layer **18**, which in one embodiment is made of a silicon oxide, resulting in a reduced space charge zone in the semiconductor body, rather than a large part of the space charge zone occurring in the semiconductor body **6** as was previously the case with charge compensation devices. A wide space charge zone is thus reduced no further than the size of the cell field **9**, making it possible to achieve a high additional capacitance in the edge region **12**. Due to the voltage requirement of high-blocking charge compensation devices the field plate oxide layer **18** must in addition be of a minimum thickness in order to prevent field breakdowns.

[0017] A gate oxide thickness d_G is not therefore suitable for high blocking voltages and as a result in this embodiment, the field plate oxide layer **18** between the upper side **7** of the semiconductor body **6** and the field plate positioned on the field plate oxide layer **18**, which is made of polycrystalline silicon, for example, is significantly thicker than the gate oxide **19**. Alternatively, it is even possible to apply the intermediate insulating layer thickness d_z of the central cell field **9** in the edge region **12** in order to position the capacitance-increasing field plate **15** in the edge region **12** and, for example, to make it of a metal. n-doping in the semiconductor body **6** in the edge region **12** of a few 10^{15} cm^{-3}, for example 4×10^{15} cm^{-3}, and a field plate oxide layer thickness d_F of up to a few micrometers, for example 2.3 μm, result in a space charge zone of approximately 2 μm in the edge region **12**, and in a semiconductor body **6** made of silicon a gate-drain voltage V_{GD} of 100 V drops by approximately 12 V.

[0018] If, for example, the gate bond contact area **13** has an edge length within a range of approximately 0.2 mm to approximately 1 mm, i.e., for example a surface area of 0.438×0.353 mm^2, it is possible with a transition region **30** of approximately 50 μm to raise the potential at all four edges **29** in the edge region **12** of the semiconductor body **6**, and in each case to achieve an effective area for the additional capacitance with the aid of the capacitance-increasing field plate within a range of approximately 0.1 mm to approximately 0.94 mm, i.e., for example a surface area of 0.338×0.253 mm^2, giving an additional capacitance in the region of up to several picofarad, e.g., 1 pF picofarad, at a gate voltage of 100 V.

[0019] This semiconductor element **1** illustrated in FIG. **1** involves no additional production costs. It is possible to go on using mask processes as in the past. Moreover, it is not necessary to enlarge the chip area in order to create additional reverse transfer capacitance through the field plate **15** in the edge region **12**. Furthermore, by coupling the field plate **15** to the gate bond contact area **13** by a contact via **16**, the additional capacitance thus created is dependent on the drain source voltage V_{DS} to only a slight extent and is therefore effective in a range in which reverse transfer capacitance C_{GD} is small.

[0020] In order to make use of this it is simply necessary to create the transition region **30** from the column regions/charge compensation zones **22** with columns of the cell field **9** to the edge regions **12** as indicated in the structures illustrated in the following figures. To this end, as illustrated in FIG. **1**, the compensation charge of the columns **20** is reduced bit by bit starting from cell field **9** until finally only one n-doped region remains in the edge region **12**. In addition, the vertical distribution of the doping in the charge compensation columns **22** can be varied. It is also possible to reduce the p-column width b bit by bit, as illustrated in FIG. **1**, from b_1 via b_2 to b_3. Similarly, where further areas are available in the edge region **12** on the upper side **7** of the semiconductor body **6**, it is possible to provide further gate bond contact areas **13** in order to further increase reverse transfer capacitance.

[0021] Moreover, in one embodiment in order to increase the capacitance in the edge region **12** it is possible to further reduce the thickness of the field plate oxide layer **18**, i.e., the thickness of an oxide between the polysilicon of the gate and the silicon surface **7** in the region of the gate bond contact area **13**, particularly since in theory an oxide thickness of 0.6 μm is sufficient for a dielectric strength of 600 V. In order to meet critical reliability requirements, it is thus useful to provide a double oxide thickness of 1.2 μm.

[0022] It may be useful to select a thickness of field plate oxide layer **18** in the region of the field plate **15** different from that of the oxide layer outside the region of the field plate in order to optimise the oxide thickness in these regions in accordance with the requirements for a flange, for example. If the thickness outside the field plate **15** is approximately 2.4 μm, for example, and if it is reduced to 1.2 μm in the region of the field plate **15** in accordance with the consideration set out above, it is possible to increase reverse transfer capacitance in relation to the homogeneous, greater thickness. As a result, it would be possible—discounting the decrease in voltage in the semiconductor material—to increase the value of 1 pF cited above by a factor of 2, to 2 pF.

[0023] A process for the production of a semiconductor device **1** with a charge carrier structure **5** in a semiconductor body **6** including an upper side **7** and a lower side **8** can be carried out with the following processes. Following the completion of drift zones **26** and charge compensation zones **22** on a semiconductor body **6** which takes the form of a semiconductor wafer, and following the application of a gate oxide **19** in the cell field **9** a field plate oxide layer **18** thicker than the gate oxide **19** is applied in the edge region **12**. An electrically conductive, capacitance-increasing field plate structure **15** is then applied to the field plate oxide layer **18**. This can take place simultaneously with the application of gate electrode material **28** in the cell field **9**.